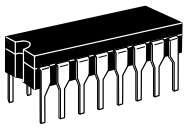
MC14043B
MC14044B

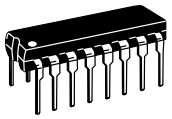
CMOS MSI
Quad R–S Latches

The MC14043B and MC14044B quad R–S latches are constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

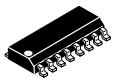
- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Outputs Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



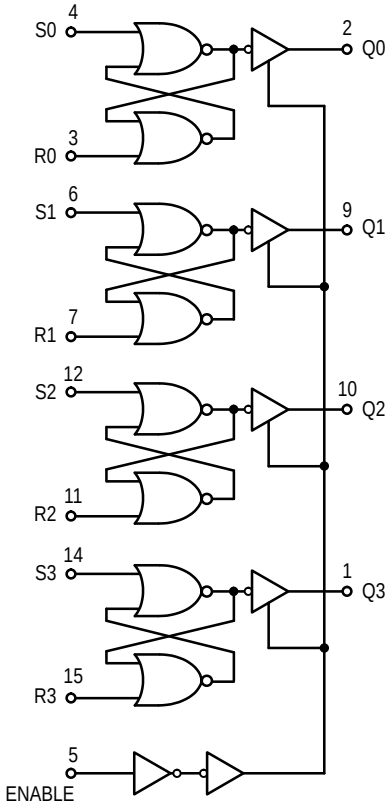
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

MC14043B



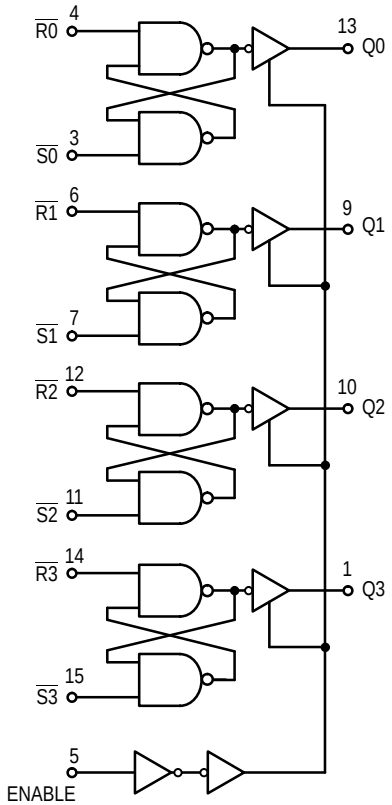
V_{DD} = PIN 16
V_{SS} = PIN 8
NC = PIN 13

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don’t Care

MC14044B



V_{DD} = PIN 16
V_{SS} = PIN 8
NC = PIN 2

TRUTH TABLE

$\overline{S}$	$\overline{R}$	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don’t Care

REV 3
1/94

ELECTRICAL CHARACTERISTICS (Vottages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level Vin = VDD or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (VD = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(VD = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(VD = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (VD = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(VD = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(VD = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	µAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (CL = 50 pF on all outputs all buffers switching)	I_T	5.0 10 15	I_T = (0.58 µA/kHz) f + I_{DD} I_T = (1.15 µA/kHz) f + I_{DD} I_T = (1.73 µA/kHz) f + I_{DD}							µAdc
Three–State Output Leakage Current	I_{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential Performance.

"The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = iT(50\ pF) + (CL - 50)\ Vfk$$

where: IT is in µA (per package), CL in pF, V = (VDD − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

. Maximum Ratings are those values beyond which darnage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages − 12 mW/°C From 100°C To 125°C

MAXIMUM RATINGS* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which darnage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against darnage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper Operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le$ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or VDD). Unused Outputs must be left open.

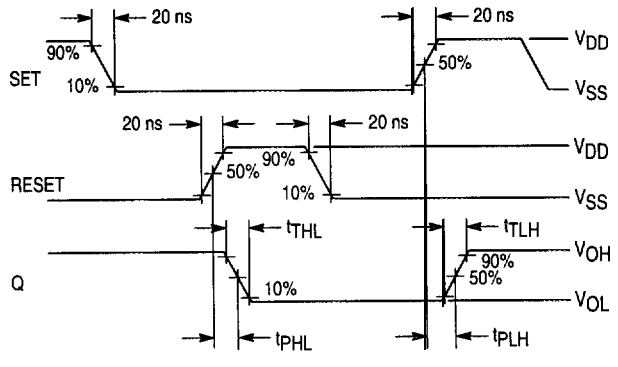
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	VDD Vdc	Min	TYP #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 32.5 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.90 ns/pF) C_L + 130 ns		5.0	—	175	350	
t_{PLH} = (0.36 ns/pF) C_L + 57 ns		10	—	75	175	
t_{PLH} = (0.26 ns/pF) C_L + 47 ns		15	—	60	120	
t_{PHL} = (0.90 ns/pF) CL + 130 ns	t_{PHL}	5.0	—	175	350	ns
t_{PHL} = (0.90 ns/pF) CL + 57 ns		10	—	75	175	
t_{PHL} = (0.26 ns/pF) CL + 47 ns		15	—	60	120	
Set, Set Pulse Width	t_W	5.0	200	60	—	ns
		10	100	40	—	
		15	70	30	—	
Reset, $\overline{\text{Reset}}$ Pulse Width	t_W	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Three–State Enable/Disable Delay	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5.0	—	150	300	ns
		10	—	80	160	
		15	—	55	110	

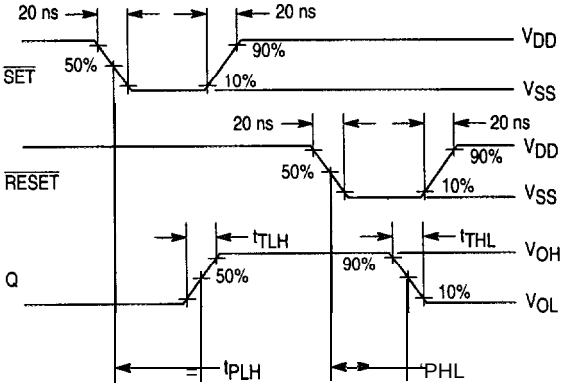
* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential Performance.

AC WAVEFORMS

MC14043B



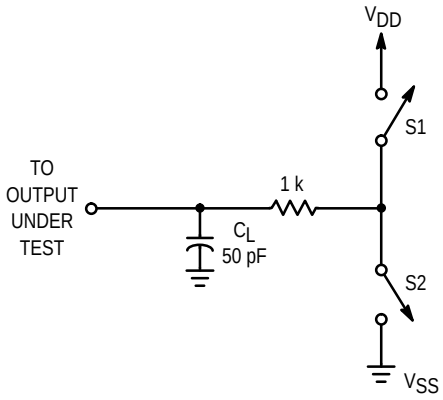
MC1 40448

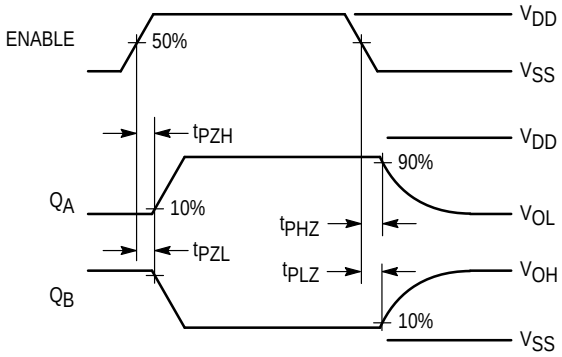


THREE–STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3–State Tests

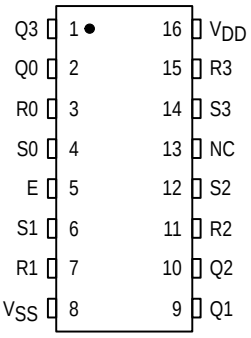
Test	Enable	S1	S2	Q	MC14043B		MC14044B	
					S	R	$\overline{S}$	$\overline{R}$
t_{PZH}	⌐	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PZL}	⌐	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}
t_{PHZ}	¬	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PLZ}	¬	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}



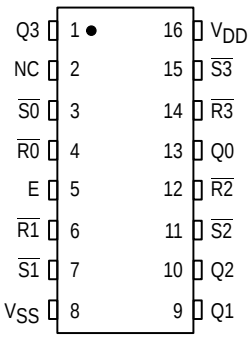


PIN ASSIGNMENT

MC14043B



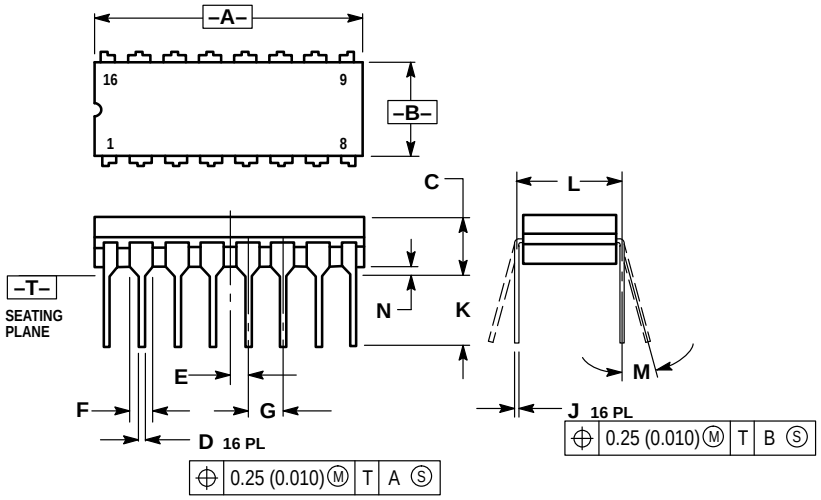
MC14044B



NC = NO CONNECTION

OUTLINE DIMENSIONS

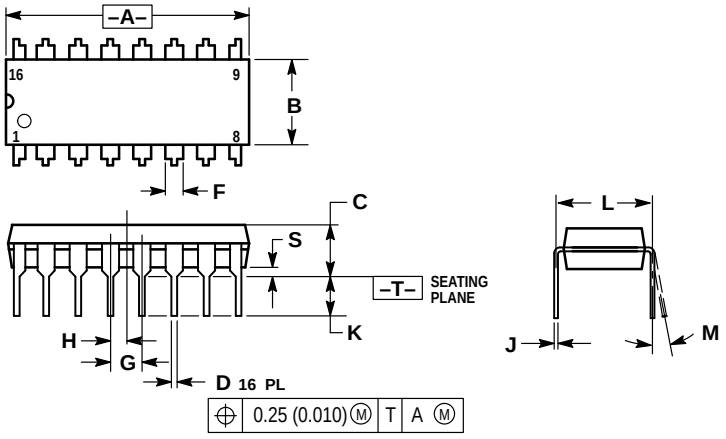
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

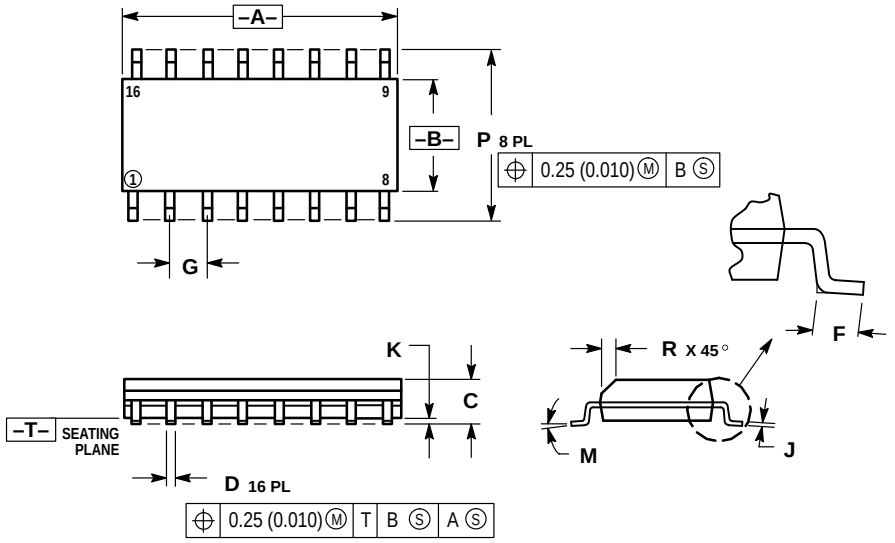


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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