CMOS MSI

Quad R-S Latches

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- **Double Diode Input Protection**
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

MC14043B MC14044B



L SUFFIX CERAMIC CASE 620



P SUFFIX PLASTIC CASE 648

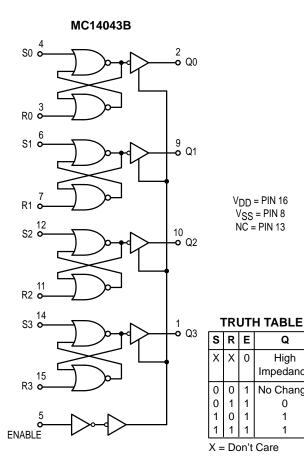


D SUFFIX SOIC CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic MC14XXXBCL Ceramic MC14XXXBD SOIC

 $T_{\Delta} = -55^{\circ}$ to 125°C for all packages.



R0 • <u>₹</u> 3 R1 6 9 Q1 S1 o R2 0-10 • Q2 <u>S2</u> 11 **○**-R3 **0 o** Q3

High Impedance

No Change

0

1

ENABLE

MC14044B

V_{DD} = PIN 16 V_{SS} = PIN 8 NC = PIN 2

TRUTH TABLE

| S | R | Ε | Q |
|---|---|---|-----------|
| Χ | Χ | 0 | High |
| | | | Impedance |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | No Change |

X = Don't Care

ELECTRICAL CHARACTERISTICS (Vottages Referenced to V_{SS})

| | | V _{DD} | - 55 | 5°C | | 25°C | | 125 | °C | |
|---|-----------------|-------------------------|-----------------------------------|----------------------|-----------------------------------|---|----------------------|---------------------------|----------------------|------|
| Characteristic | Symbol | Vdc | Min | Max | Min | Тур# | Max | Min | Max | Unit |
| Output Voltage "0" Level Vin = VDD or 0 | V _{OL} | 5.0 10 15 | | 0.05 0.05 0.05 | _ _ _ | 0 0 0 | 0.05 0.05 0.05 | | 0.05 0.05 0.05 | Vdc |
| v_{in} = 0 or v_{DD} | Voн | 5.0 10 15 | 4.95 9.95 14.95 | | 4.95 9.95 14.95 | 5.0 10 15 | - - | 4.95 9.95 14.95 | _ | Vdc |
| Input Voltage "0" Level (VD = 4.5 or 0.5 Vdc) (VD = 9.0 or 1.0 Vdc) (VD = 13.5 or 1.5 Vdc) | VIL | 5.0 10 1 5 | | 1.5 3.0 4.0 | | 2.25 4.50 6.75 | 1.5 3.0 4.0 | | 1.5 3.0 4.0 | Vdc |
| "1" Level (VD = 0.5 or 4.5 Vdc) (VD = 1.0 or 9.0 Vdc) (VD = 1.5 or 13.5 Vdc) | ∨н | 5.0 10 15 | 3.5 7.0 11 | | 3.5 7.0 11 | 2.75 5.50 8.25 | | 3.5 7.0 11 | 1 1 1 | Vdc |
| Output Drive Current (VOH = 2.5 Vdc) Source (VOH = 4.6 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vdc) | ЮН | 5.0 5.0 10 15 | - 3.0 - 0.64 - 1.6 - 4.2 | | - 2.4 - 0.51 - 1.3 - 3.4 | - 4.2 - 0.88 - 2.25 - 8.8 | | 1.7 0.36 0.9 2.4 | I I I I | mAdc |
| $(V_{OL} = 0.4 \text{ Vdo})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$ | loL | 5.0 10 15 | 0.64 1.6 4.2 | _ | 0.51 1.3 3.4 | 0.88 2.25 8.8 | <u>-</u> - | 0.36 0.9 2.4 | | mAdc |
| Input Current | lin | 15 | | ± 0.1 | | ±0.00001 | ± 0.1 | | ± 1.0 | μAdc |
| Input Capacitance (V _{in} = 0) | C _{in} | | | ! <u></u> | | 5.0 | 7.5 | | _ | pF |
| Quiescent Current (Per Package) | IDD | 5.0 10 15 | | 1.0 2.0 4.0 | _ | 0.002 0.004 0.006 | 1.0 2.0 4.0 | - | 30 60 120 | μAdc |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) (CL = 50 pF on all outputs all buffers switching) | ¹T | 5.0 10 15 | | | $1_{T} = (1$ | .58 μΑ/kHz) .15 μΑ/kHz) .73 μΑ/kHz) | f + I _{DD} | | | μAdc |
| Three-State Output Leakage Current | lTL | 15 | - | ± 0.1 | _ | ± 0.0001 | ± 0.1 | | ± 3.0 | μAdc |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential Performance.

$$i_T(C_L) = iT(50 pF) + (CL - 50) Vfk$$

where: IT is in μA (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.004.

[&]quot;The formulas given are for the typical characteristics only at 25°C.

[†]To calculate total supply current at loads other than 50 pF:

[•] Maximum Ratings are those values beyond which damage to the device may occur.

[†]Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages - 12 mW/°C From 100°C To 125°C

MAXIMUM RATINGS* (Voltages Referenced to VSS)

| Symbol | Parameter | Value | Unit |
|------------------------------------|--|--------------------------------|------|
| V _{DD} | DC Supply Voltage | - 0.5 to + 18.0 | ٧ |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | - 0.5 to V _{DD} + 0.5 | V |
| l _{in} , l _{out} | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| P_{D} | Power Dissipation, per Package† | 500 | mW |
| Tstg | Storage Temperature | - 65 to + 150 | °C |
| ΤL | Lead Temperature (8-Second Soldering) | 260 | °C |

^{*} Maximum Ratings are those values beyond which darnage to the device may occur. †Temperature Derating:

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

This device contains protection circuitry to guard against darnage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper Operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ VDD.

Unused inputs must always be tied to an

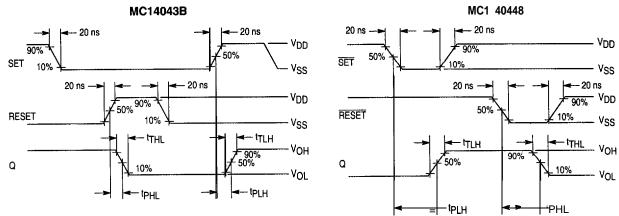
appropriate logic voltage level (e.g., either VSS or VDD). Unused Outputs must be left open.

| Characteristic | Symbol | VDD Vdc | Min | Typ# | Max | Unit |
|--|---------------------------------|-----------------|------------------|-----------------|-------------------|------|
| Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ | ⁴т∟н | 5.0 10 15 | | 100 50 40 | 200 100 80 | ns |
| Output Fall Time t _{THL} = (1.35 ns/pF) C _L + 32.5 ns t _{THL} = (0.60 ns/pF) C _L + 20 ns t _{THL} = (0.40 ns/pF) C _L + 20 ns | ţтнL | 5.0 10 15 | - | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time tpLH = (0.90 ns/pF) C _L + 130 ns tpLH = (0.36 ns/pF) C _L + 57 ns tpLH = (0.26 ns/pF) C _L + 47 ns | †PLH | 5.0 10 15 | | 175 75 60 | 350 175 120 | ns |
| tpHL = (0.90 ns/pF) CL + 130 ns tpHL = (0.90 ns/pF) CL + 57 ns tpHL = (0.26 ns/pF) CL + 47 ns | †PHL | 5.0 10 15 | = | 175 75 60 | 350 175 120 | ns |
| Set, Set Pulse Width | tW | 5.0 10 15 | 200 100 70 | 60 40 30 | | ns |
| Reset, Reset Pulse Width | tw | 5.0 10 15 | 200 100 70 | 80 40 30 | | ns |
| Three-State Enable/Disable Delay | tplz, tpHz, tpZL, tPZH | 5.0 10 15 | = | 150 80 55 | 300 160 110 | ns |

^{*} The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential Performance.

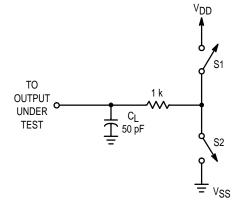
AC WAVEFORMS

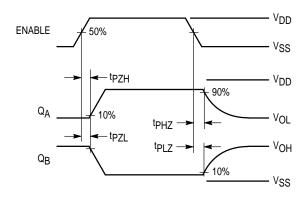


THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3-State Tests

| | | | | | MC14043B | | MC14044B | |
|------------------|--------|--------|--------|---|----------|----------|----------|----------|
| Test | Enable | S1 | S2 | Q | S | R | S | R |
| ^t PZH | | Open | Closed | Α | V_{DD} | VSS | VSS | V_{DD} |
| t _{PZL} | | Closed | Open | В | VSS | V_{DD} | V_{DD} | VSS |
| ^t PHZ | ~ | Open | Closed | Α | V_{DD} | VSS | VSS | V_{DD} |
| t _{PLZ} | ~ | Closed | Open | В | VSS | V_{DD} | V_{DD} | VSS |





PIN ASSIGNMENT

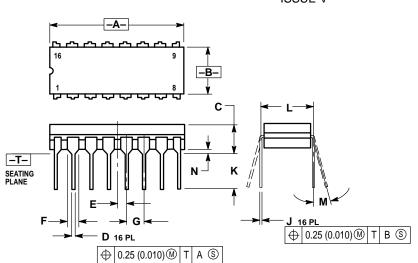
| MC14043B | | | | | | | | |
|-------------------|-----|----|--------------------------------|--|--|--|--|--|
| Q3 [| 1 ● | 16 | D _D V _{DD} | | | | | |
| Q0 [| 2 | 15 |] R3 | | | | | |
| R0 [| 3 | 14 |] S3 | | | | | |
| S0 [| 4 | 13 | NC NC | | | | | |
| E [| 5 | 12 |] S2 | | | | | |
| S1 [| 6 | 11 | R2 | | | | | |
| R1 [| 7 | 10 | Q2 | | | | | |
| V _{SS} [| 8 | 9 | Q1 | | | | | |

| MC14044B | | | | | | | |
|----------|---|-----|----|-----------------|--|--|--|
| Q3 | þ | 1 ● | 16 | V _{DD} | | | |
| NC | þ | 2 | 15 |] S3 | | | |
| S0 | þ | 3 | 14 |] R3 | | | |
| R0 | þ | 4 | | Q0 | | | |
| Ε | þ | 5 | 12 | R2 | | | |
| R1 | þ | 6 | 11 |] <u>52</u> | | | |
| S1 | þ | 7 | 10 | Q2 | | | |
| Vss | þ | 8 | 9 | Q1 | | | |

NC = NO CONNECTION

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



NOTES:

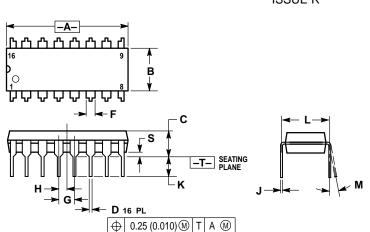
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION L TO CENTER OF LEAD WHEN
 FORMED PARALLEL.
 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC

| | INC | HES | MILLIN | IETERS | | | |
|-----|-----------|-------|----------|--------|--|--|--|
| DIM | MIN | MAX | MIN | MAX | | | |
| Α | 0.750 | 0.785 | 19.05 | 19.93 | | | |
| В | 0.240 | 0.295 | 6.10 | 7.49 | | | |
| С | | 0.200 | | 5.08 | | | |
| D | 0.015 | 0.020 | 0.39 | 0.50 | | | |
| Е | 0.050 BSC | | 1.27 BSC | | | | |
| F | 0.055 | 0.065 | 1.40 | 1.65 | | | |
| G | 0.100 | BSC | 2.54 BSC | | | | |
| Н | 0.008 | 0.015 | 0.21 | 0.38 | | | |
| K | 0.125 | 0.170 | 3.18 | 4.31 | | | |
| L | 0.300 BSC | | 7.62 BSC | | | | |
| М | 0° | 15° | 0 ° | 15° | | | |
| N | 0.020 | 0.040 | 0.51 | 1.01 | | | |

P SUFFIX PLASTIC DIP PACKAGE

CASE 648-08 ISSUE R



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

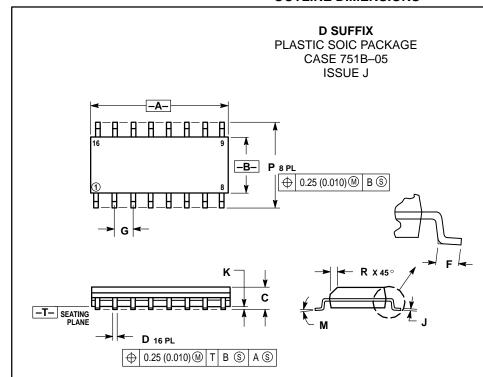
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

| | INC | HES | MILLIN | IETERS | |
|-----|-------|-------|----------|--------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 0.740 | 0.770 | 18.80 | 19.55 | |
| В | 0.250 | 0.270 | 6.35 | 6.85 | |
| С | 0.145 | 0.175 | 3.69 | 4.44 | |
| D | 0.015 | 0.021 | 0.39 | 0.53 | |
| F | 0.040 | 0.70 | 1.02 | 1.77 | |
| G | 0.100 | BSC | 2.54 BSC | | |
| Н | 0.050 | BSC | 1.27 BSC | | |
| J | 0.008 | 0.015 | 0.21 | 0.38 | |
| K | 0.110 | 0.130 | 2.80 | 3.30 | |
| L | 0.295 | 0.305 | 7.50 | 7.74 | |
| M | 0° | 10° | 0° | 10 ° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 | |

OUTLINE DIMENSIONS



- DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIN | IETERS | INCHES | | |
|-----|--------|--------|-----------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 9.80 | 10.00 | 0.386 | 0.393 | |
| В | 3.80 | 4.00 | 0.150 | 0.157 | |
| С | 1.35 | 1.75 | 0.054 | 0.068 | |
| D | 0.35 | 0.49 | 0.014 | 0.019 | |
| F | 0.40 | 1.25 | 0.016 | 0.049 | |
| G | 1.27 | BSC | 0.050 BSC | | |
| J | 0.19 | 0.25 | 0.008 | 0.009 | |
| Κ | 0.10 | 0.25 | 0.004 | 0.009 | |
| М | 0° | 7° | 0° | 7° | |
| Р | 5.80 | 6.20 | 0.229 | 0.244 | |
| R | 0.25 | 0.50 | 0.010 | 0.019 | |

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MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609 INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



