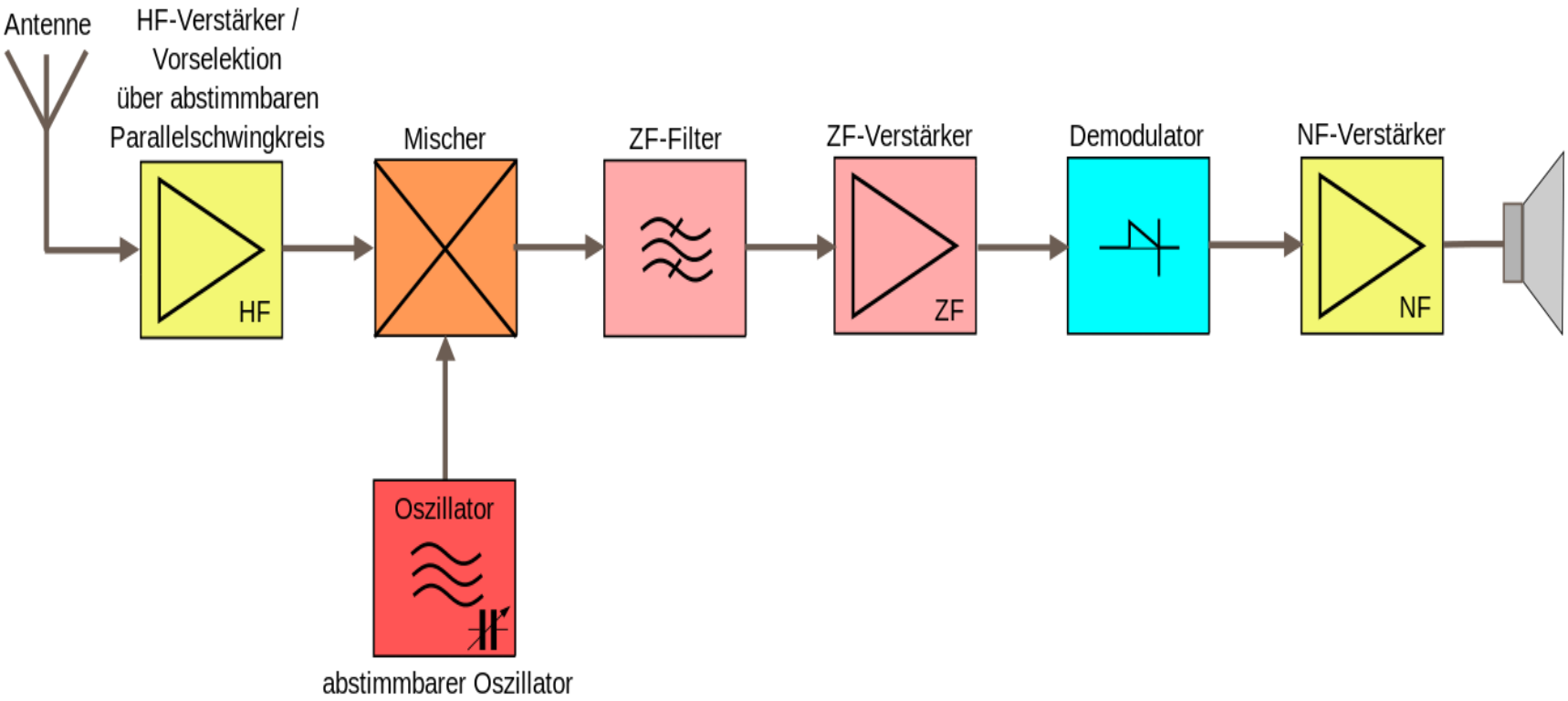
Phase-Locked-Loop (PLL)
Phasenregelkreis

PROJEKT LABOR

Gliederung

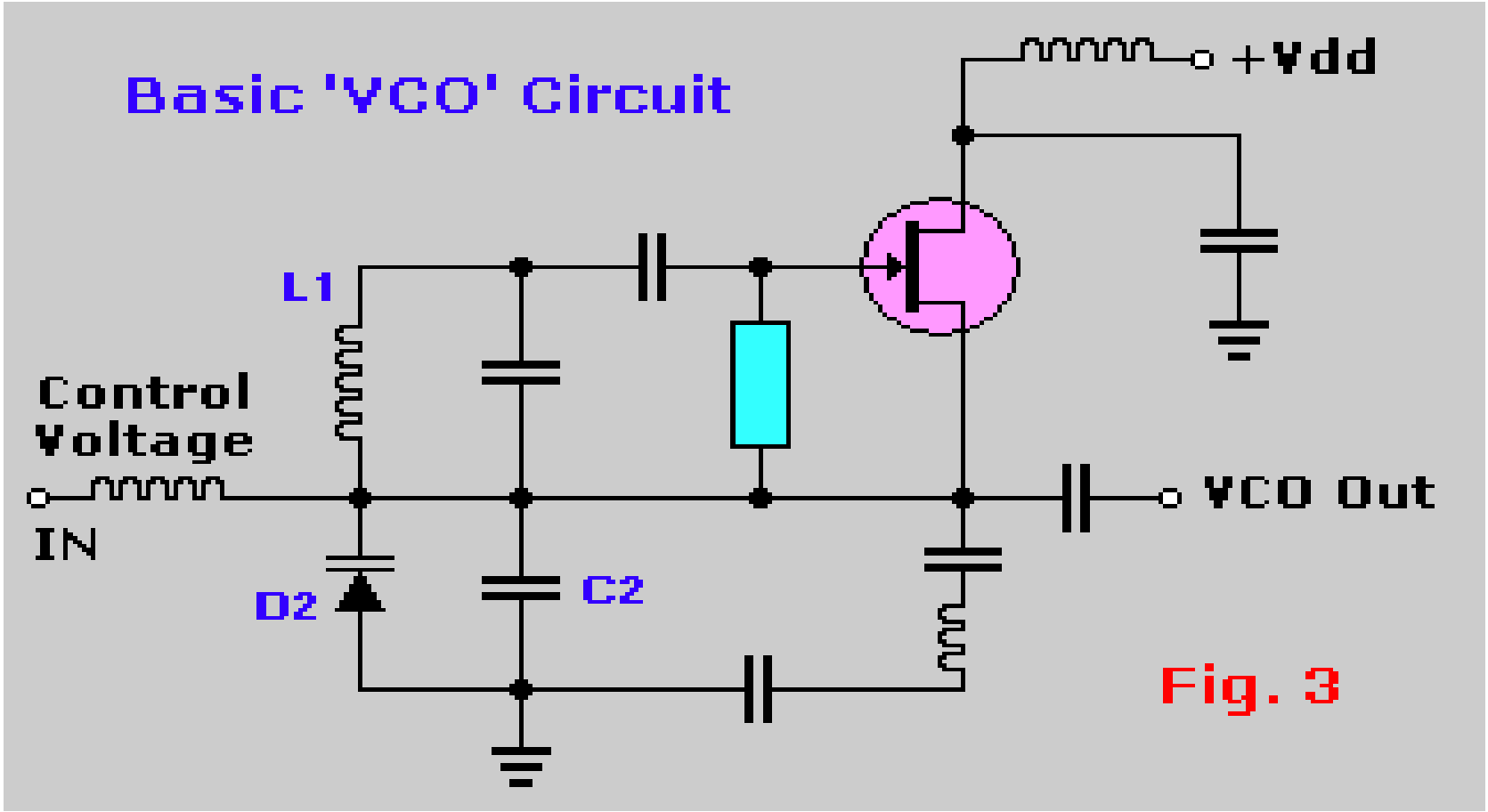
- BSB Radio
- BSB PLL
  - VCO
  - XO
  - Divider
  - PD
  - Loop-Filter
- PLL als IC

BSB Radio (Überlagerungsempfänger)



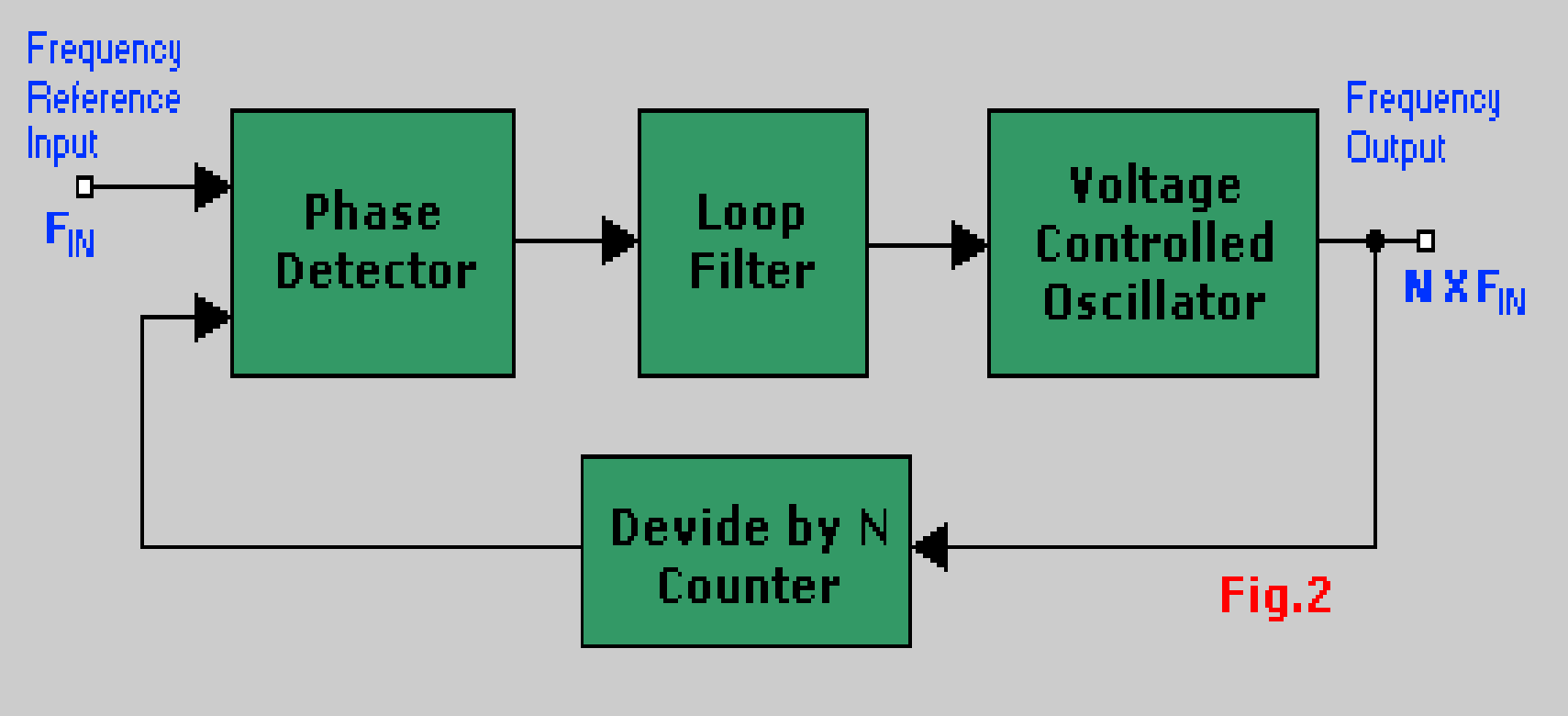
Quelle: Wikipedia – Überlagerungsampfänger

Spannungsgesteuerter Oszillator (*Voltage Controlled Oscillator VCO*)



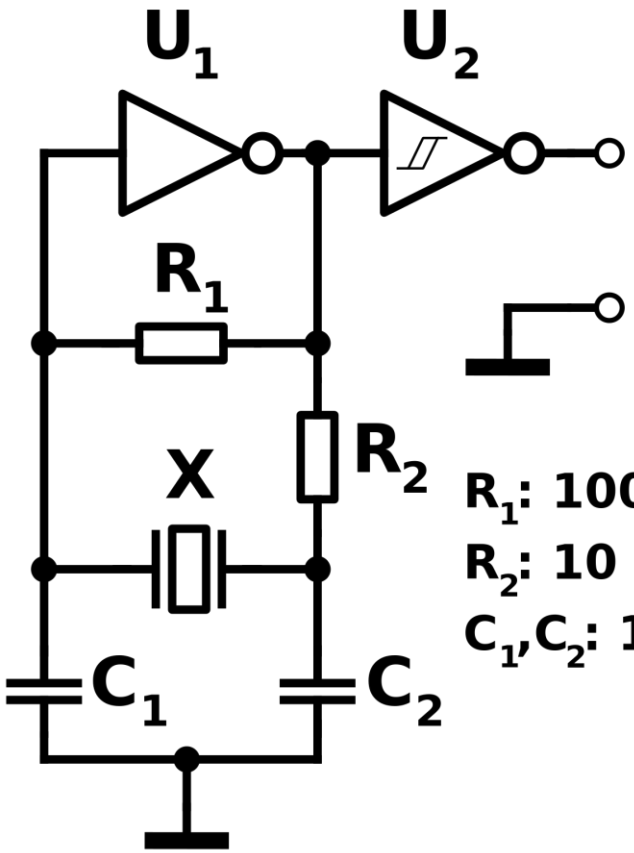
Quelle: sentex.ca – PLL

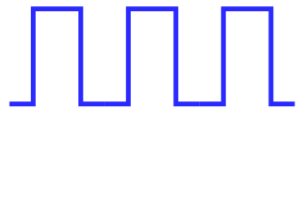
BSB Phasenregelkreis (PLL)



Quelle: sentex.ca – PLL

Quarzoszillator (XO)

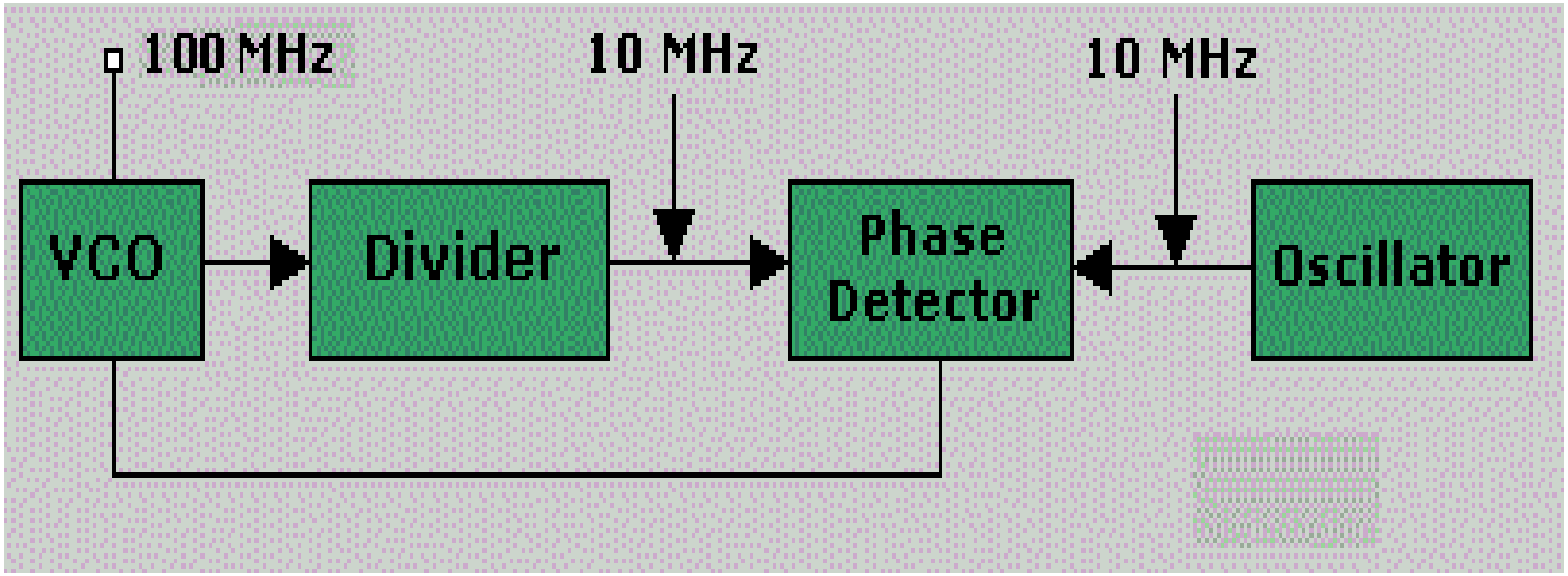




R_1: 100 kΩ … 10 MΩ
R_2: 10 Ω … 4,7 kΩ
C_1,C_2: 10 pF … 82 pF

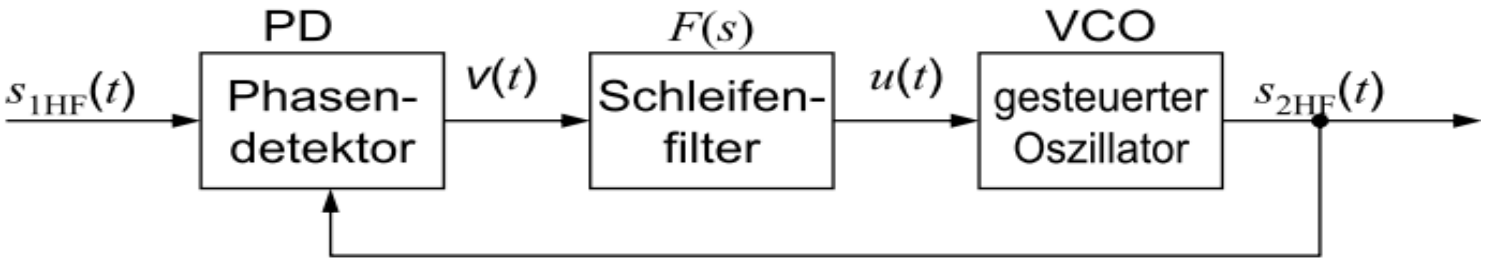
Quelle: Wikipedia – Quarzoszillator

PLL Frequenzbeispiel



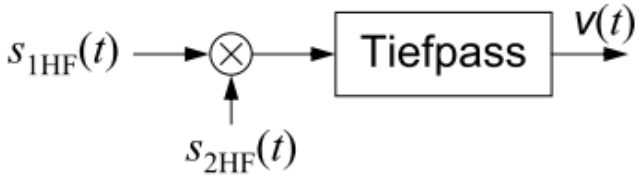
Quelle: sentex.ca - PLL

Phasendetektor (PD)



$$s_{1HF}(t) = A_1 \sin\left(\omega_0 t + \varphi_1(t)\right) + w_{HF}(t)$$

$$s_{2HF}(t) = A_2 \cos\left(\omega_0 t + \varphi_2(t)\right)$$

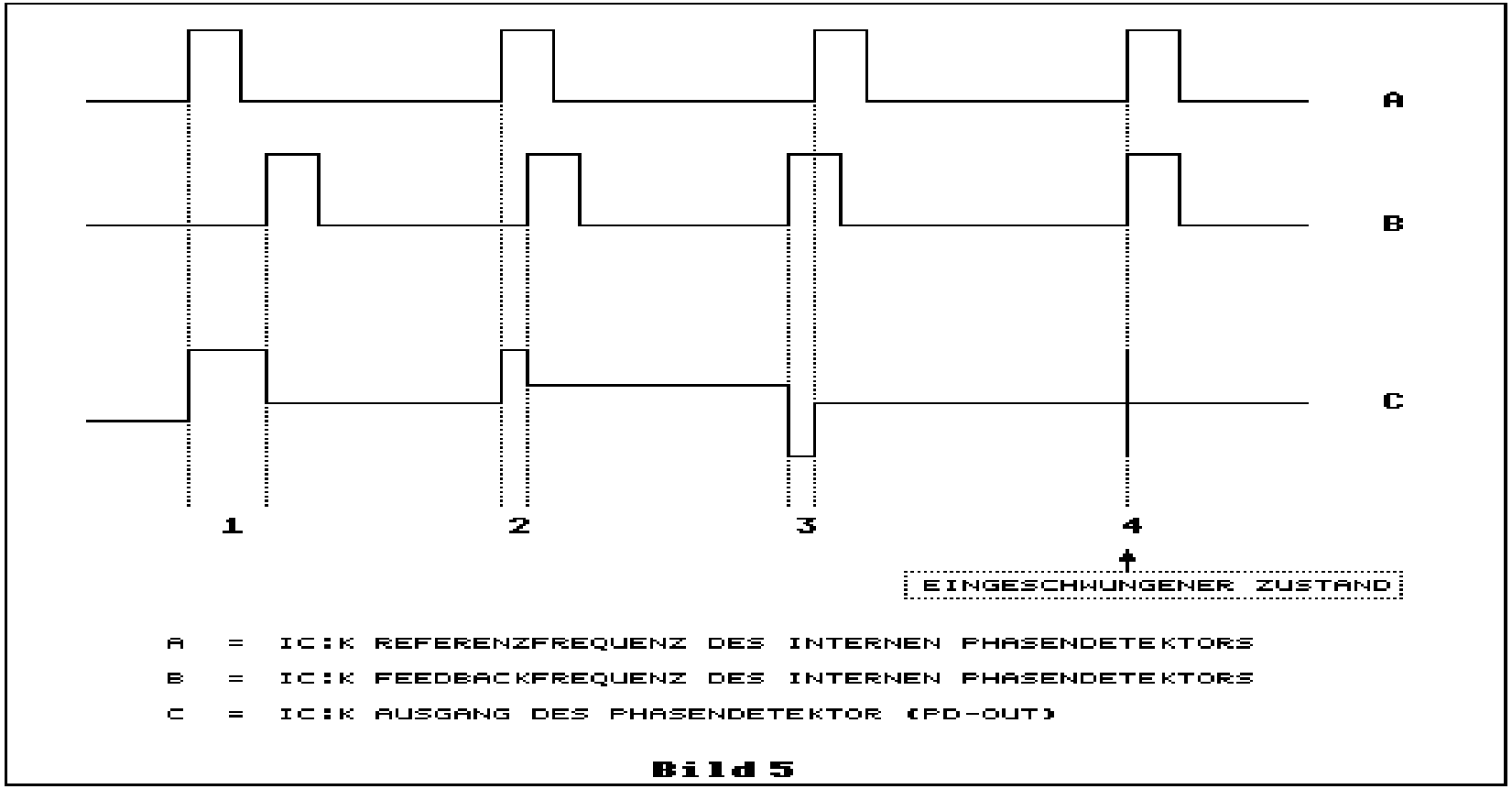


$$s_{1HF}(t) \cdot s_{2HF}(t) = A_1 A_2 \sin\left(\omega_0 t + \varphi_1(t)\right)\cos\left(\omega_0 t + \varphi_1(t)\right)$$

Additionstheorem aus der Trigonometrie: $\sin\alpha\cos\beta = \frac{1}{2}\left(\sin(\alpha-\beta)+\sin(\alpha+\beta)\right)$

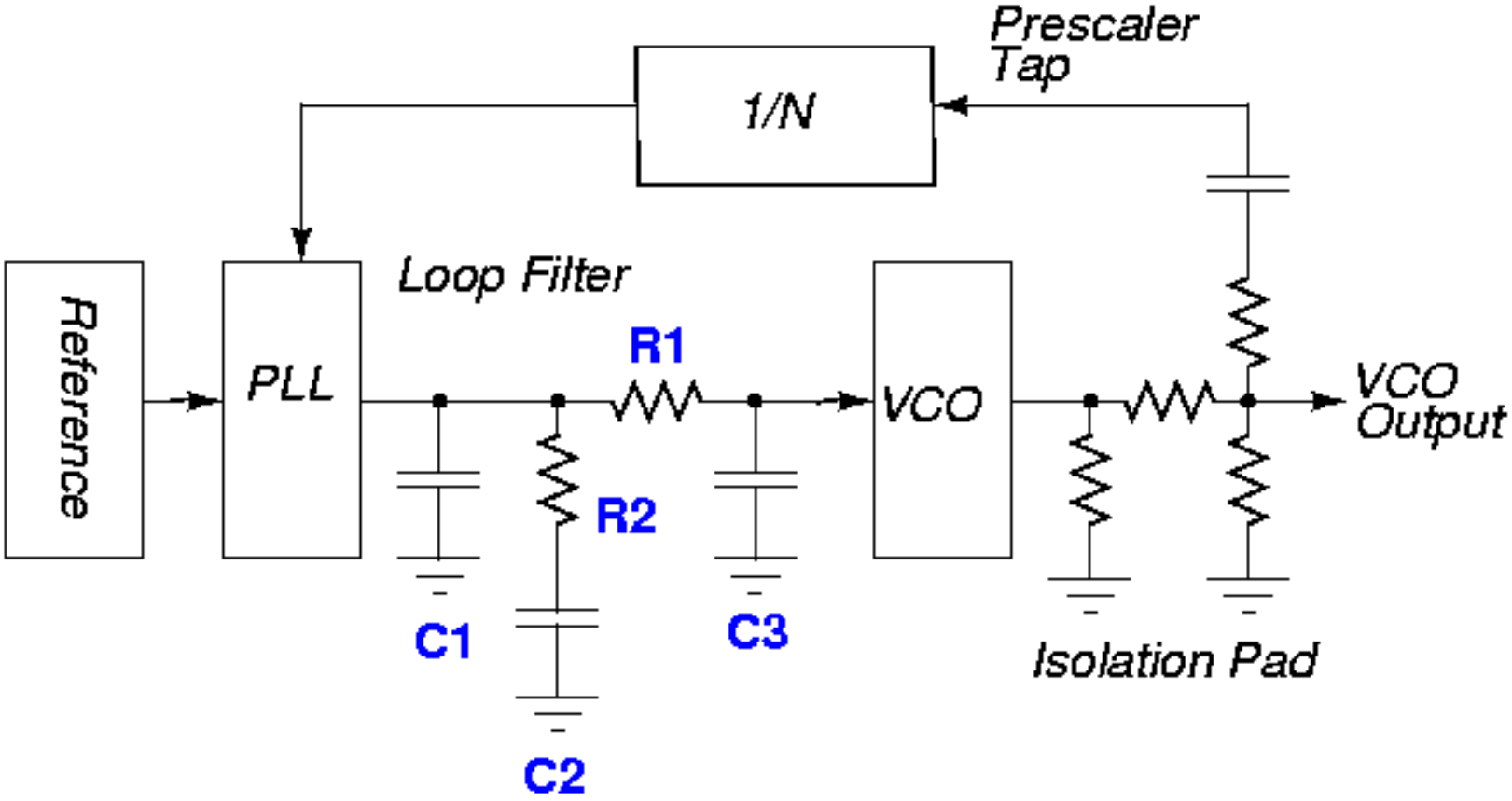
$$s_{1HF}(t) \cdot s_{2HF}(t) = \frac{A_1 A_2}{2}\left(\sin\left(\varphi_1(t)-\varphi_2(t)\right)+\sin\left(2\omega_0 t+\varphi_1(t)+\varphi_2(t)\right)\right)$$

Synchronisierung in Phase und Frequenz im PD



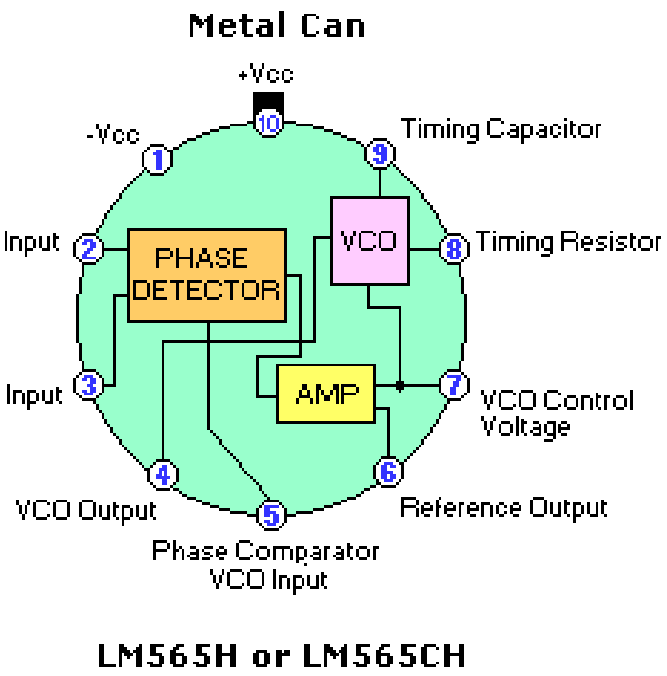
Quelle: elektronik-kompendium.de – PLL

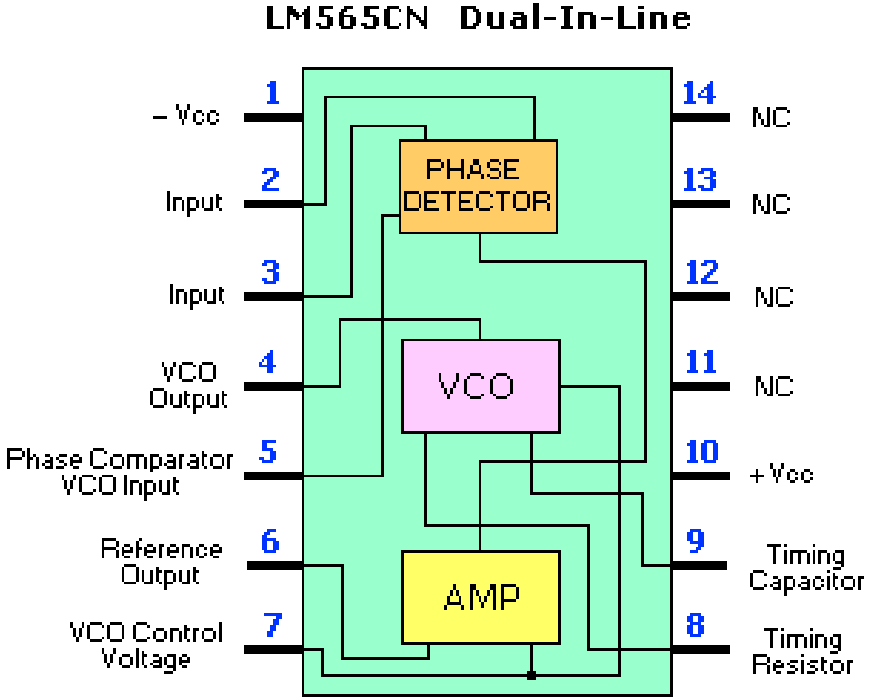
Schleifenfilter (Loop Filter)



Quelle: wetnet.net – Loop Filter

PLL als Integrierte Schaltung (IC)





Quelle: sentex.ca – PLL

Quellen

- http://www.dj4uf.de
- http://www.elektronik-kompendium.de
- http://www.sentex.ca
- Wikipedia
  - Quarzoszillator
  - Überlagerungsempfänger
  - Phasenregelkreis
  - Geradeausempfänger
  - VCO
  - Frequenzmodulation

Ende

- Vielen Dank für eure Aufmerksamkeit !