Referat über die Logikbausteine

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11.11.14

Gliederung

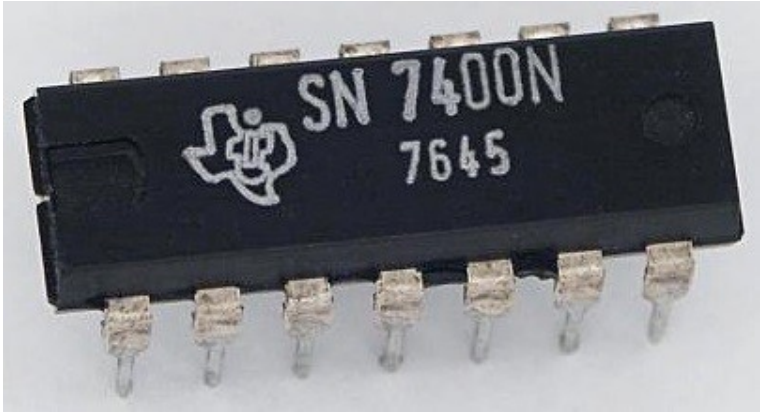
- Die Logikfamilien
- Die elementaren Logikbausteine
  - AND, OR, NOT, NAND, NOR, XOR, XNOR
  - Gatterlaufzeiten (reale und ideale) am Beispiel Inverter
- Beispiel (7-segment-Anzeige)
  - Schaltnetz für das Segment f

Was ist Logik?

Logikfamilien

TTL-Familie

- 74er Reihe



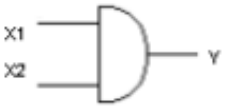
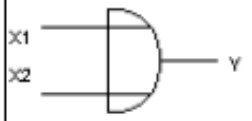
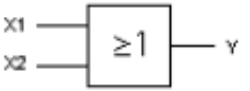
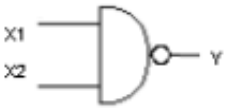
Präfix	Temperaturbereich	Bezeichnung
74'	0 °C bis +70 °C	kommerziell
84'	−40 °C bis +85 °C	industriell
54'	−55 °C bis +125 °C	militärisch

CMOS-Familie

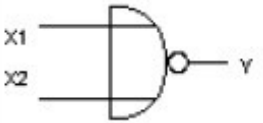
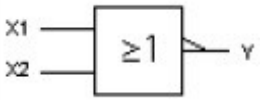
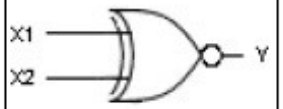
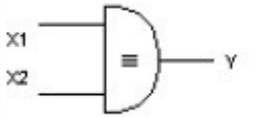
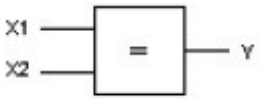
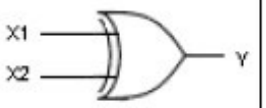
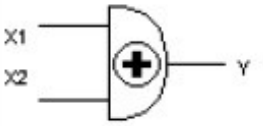
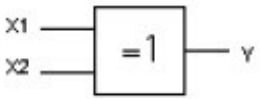
- 40er Reihe

http://www.mikrocontroller.net/articles/74xx

Die elementaren Logikbausteine

Funktion	Wahrheits-tabelle	Logik-gleichung	ANSI-Symbol (alt)	DIN-Symbol (alt)	DIN-Symbol
AND	x_1 x_2 y 0 0 0 0 1 0 1 0 0 1 1 1	$y = x_1 \wedge x_2$ $y = x_1 \cdot x_2$			
OR	x_1 x_2 y 0 0 0 0 1 1 1 0 1 1 1 1	$y = x_1 \vee x_2$ $y = x_1 + x_2$			
NAND	x_1 x_2 y 0 0 1 0 1 1 1 0 1 1 1 0	$y = \overline{x_1 \cdot x_2}$			

Die elementaren Logikbausteine

Funnktion	Wahrheits-tabelle	Logik-gleichung	ANSI-Symbol (alt)	DIN-Symbol (alt)	DIN-Symbol
NOR	x_1 x_2 y 0 0 1 0 1 0 1 0 0 1 1 0	$y = \overline{x_1 + x_2}$			
XNOR (Äquivalenz)	x_1 x_2 y 0 0 1 0 1 0 1 0 0 1 1 1	$y = x_1 \oplus x_2 =$ $x_1 \cdot x_2 + \overline{x_1} \cdot \overline{x_2}$			
XOR (Antivalenz)	x_1 x_2 y 0 0 0 0 1 1 1 0 1 1 1 0	$y = x_1 \equiv x_2 =$ $x_1 \cdot \overline{x_2} + \overline{x_1} \cdot x_2$			

Ideale und reale Gatter

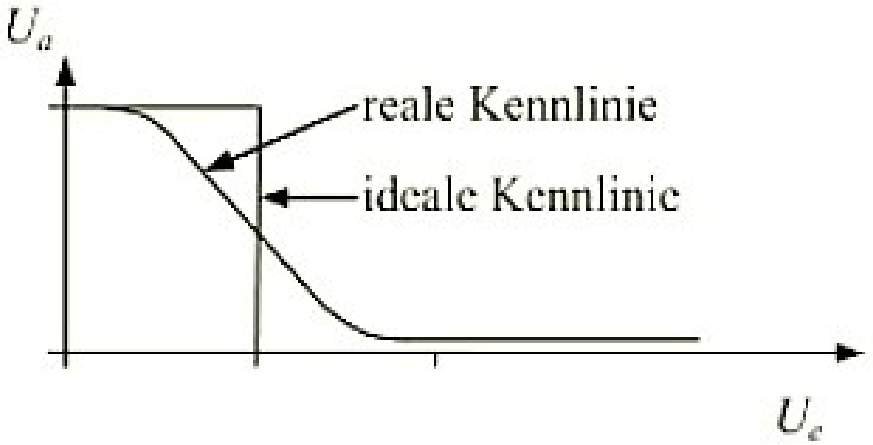
Verhalten logischer Gatter

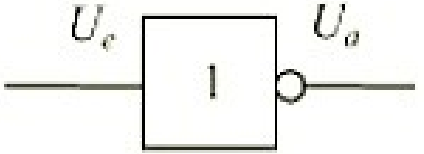
- Nur zwei Spannungspegel: **high (H)** und **low (L)**
- 1 und 0 werden den unterschiedlichen Spannungswerten zugeteilt
- Positive Logik: wenn 1 an hoher Spannung anliegt
- Negative Logik: wenn 0 an hoher Spannung anliegt

Spannung	Pegel	Logischer Zustand	
		positive Logik	negative Logik
≈ 5V	H	1	0
≈ 0V	L	0	1

Abb.: Zuordnung logischer Zustände zu den unterschiedlichen Spannungspegeln

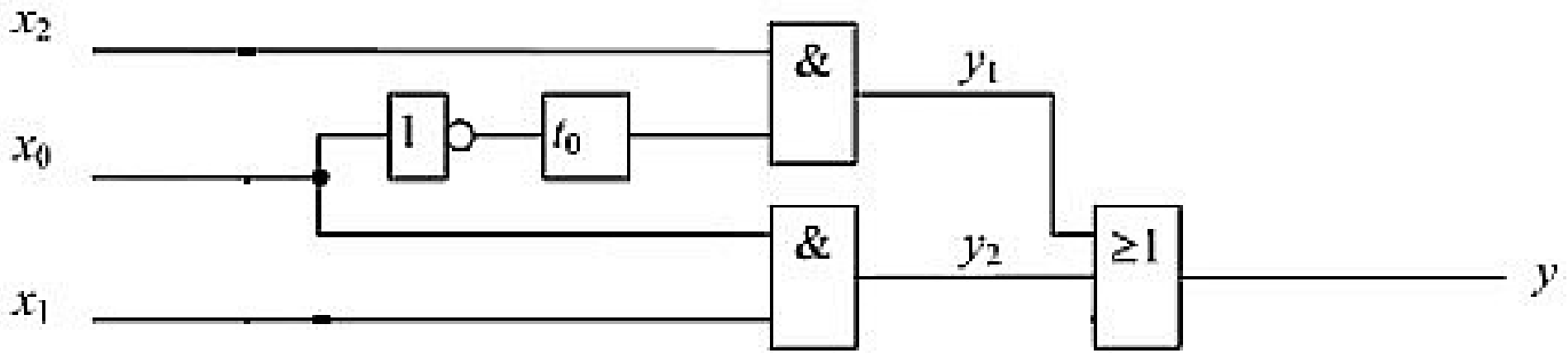
Ideale und reale Gatter





- Übertragungskennlinie kennzeichnet das Amplitudenverhalten eines Inverters
- Reale Kennlinie berücksichtigt die Laufzeit
- Laufzeit abhängig von Temperatur und fertigungsbedingte Streuung

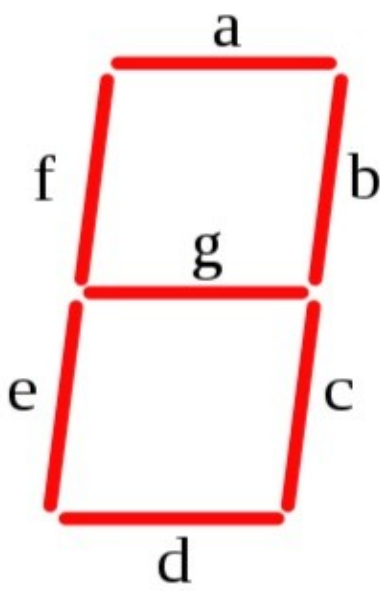
Ideale und reale Gatter



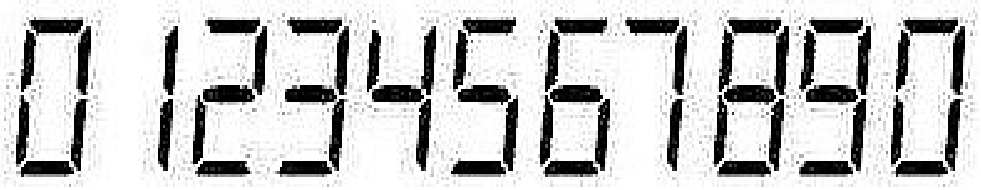
$$y = x_1 x_0 \vee x_2 \neg x_0$$

- Zusätzliches Bauteil verzögert Laufzeit an oberem AND-Gatter
  - ➔ Signal y_1 kommt mit Verzögerung t_0 gegenüber y_2 am OR-Gatter an

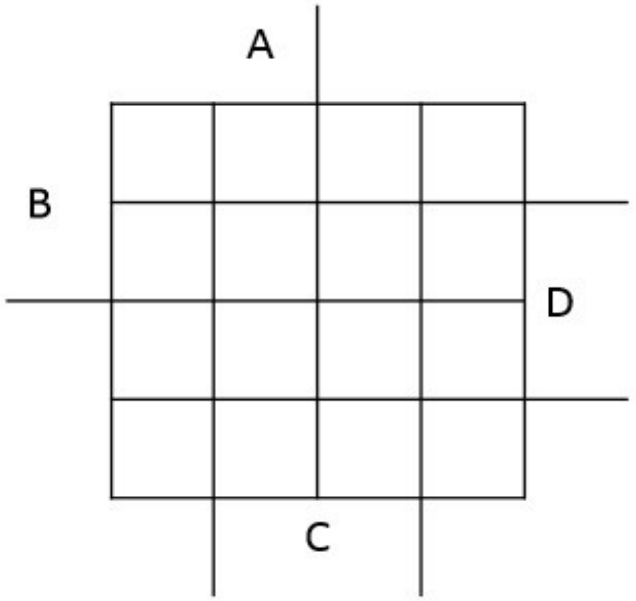
Beispiel: 7-segment-Anzeige



Dez	D	C	B	A	f
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1

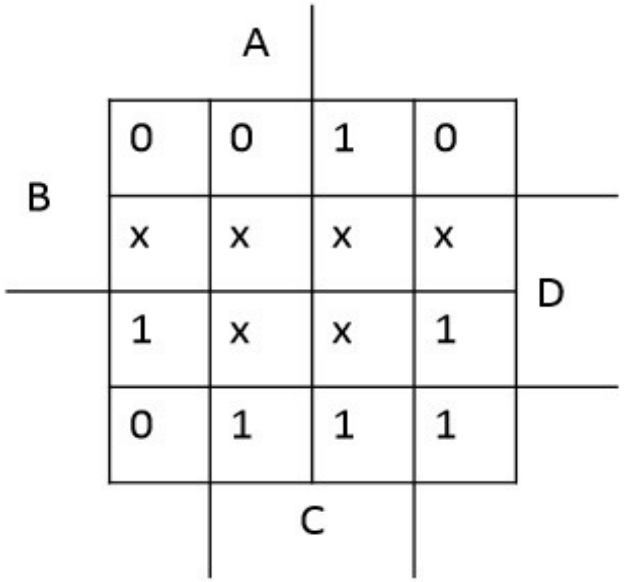


Beispiel: 7-segment-Anzeige



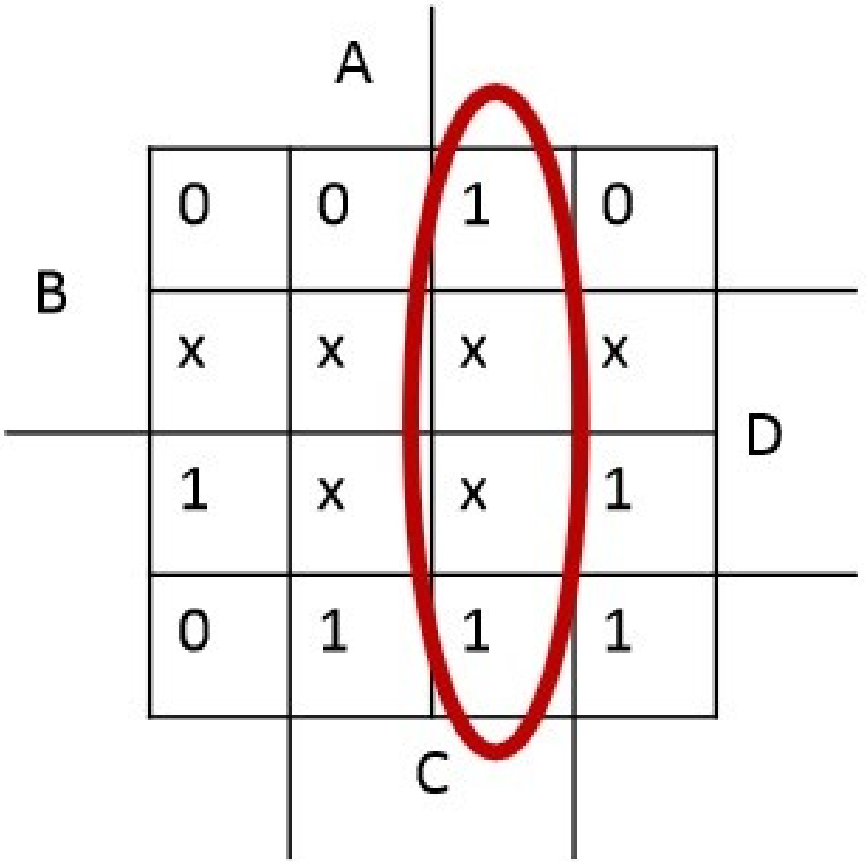
D	C	B	A	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

Beispiel: 7-segment-Anzeige



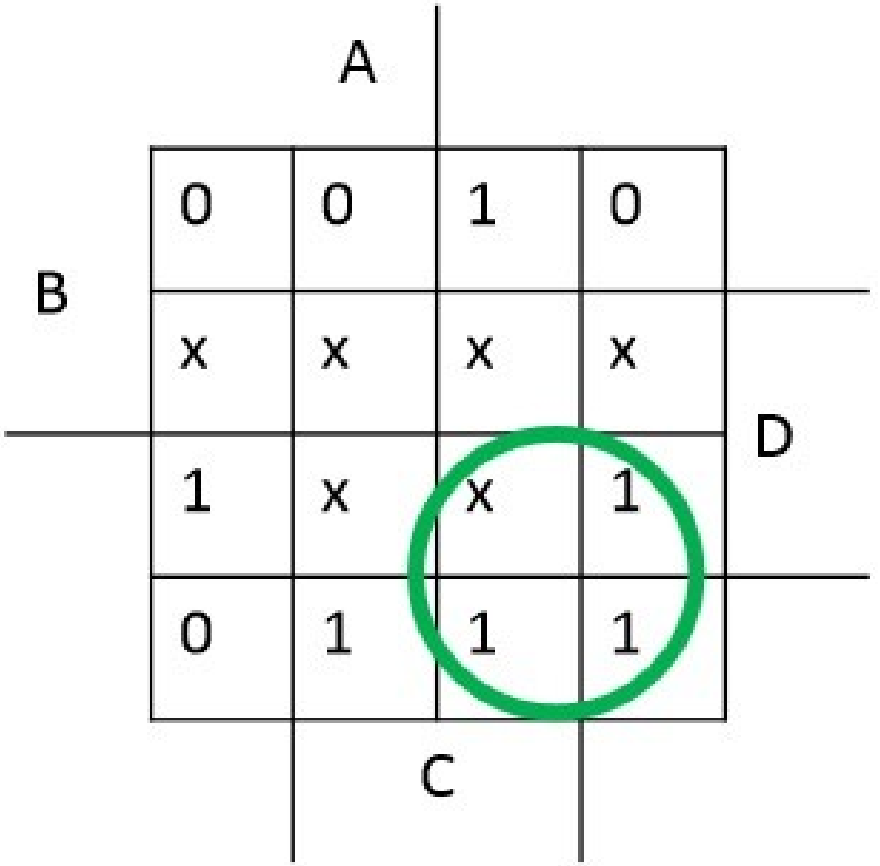
D	C	B	A	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

Beispiel: 7-segment-Anzeige



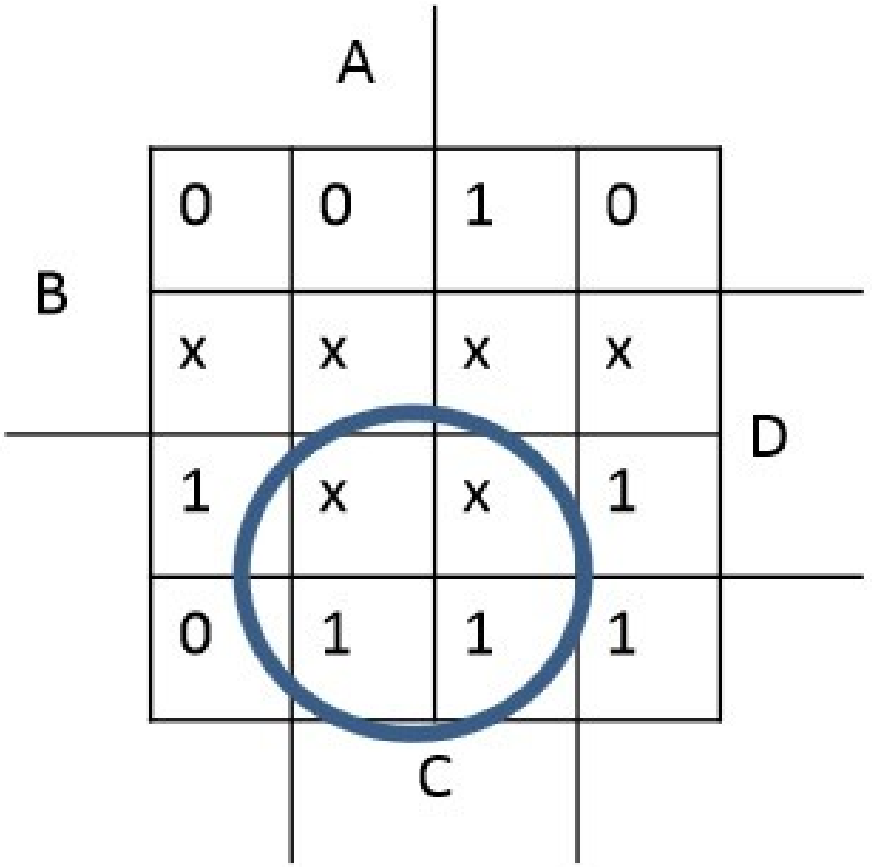
f =

Beispiel: 7-segment-Anzeige



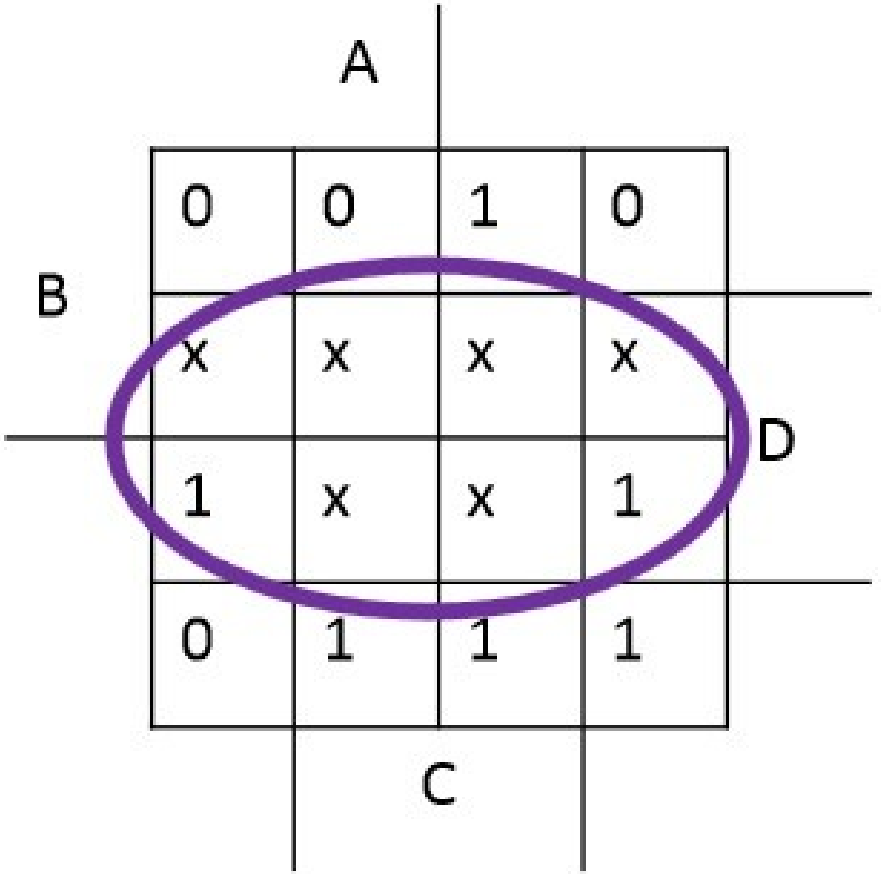
f = ¬A * C

Beispiel: 7-segment-Anzeige



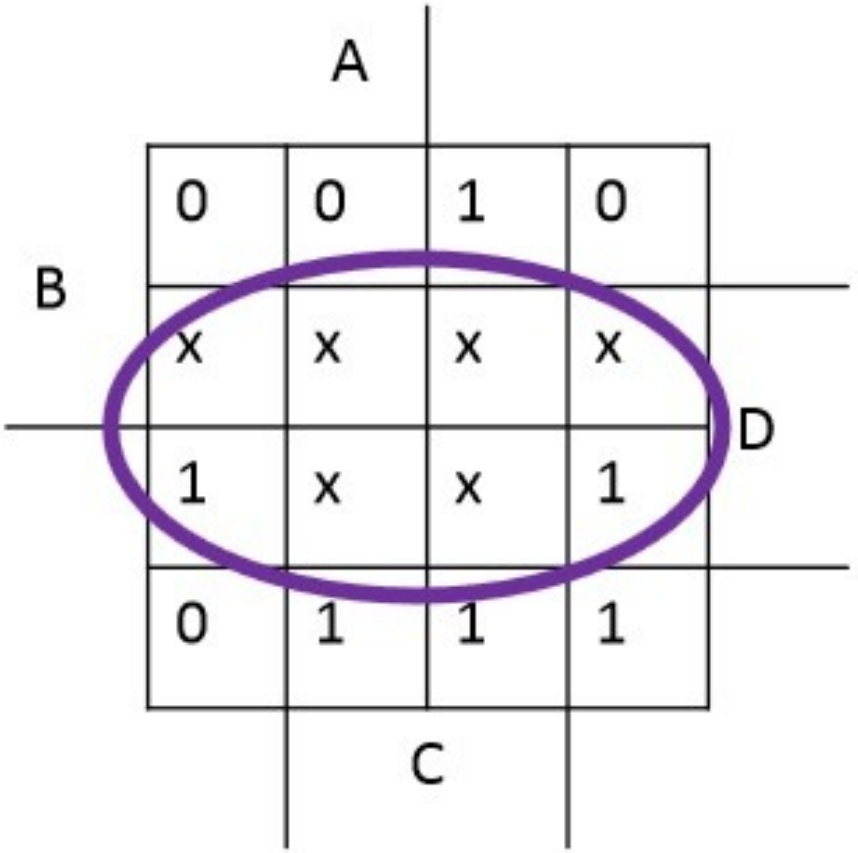
f = ¬A * C + ¬A * ¬D

Beispiel: 7-segment-Anzeige



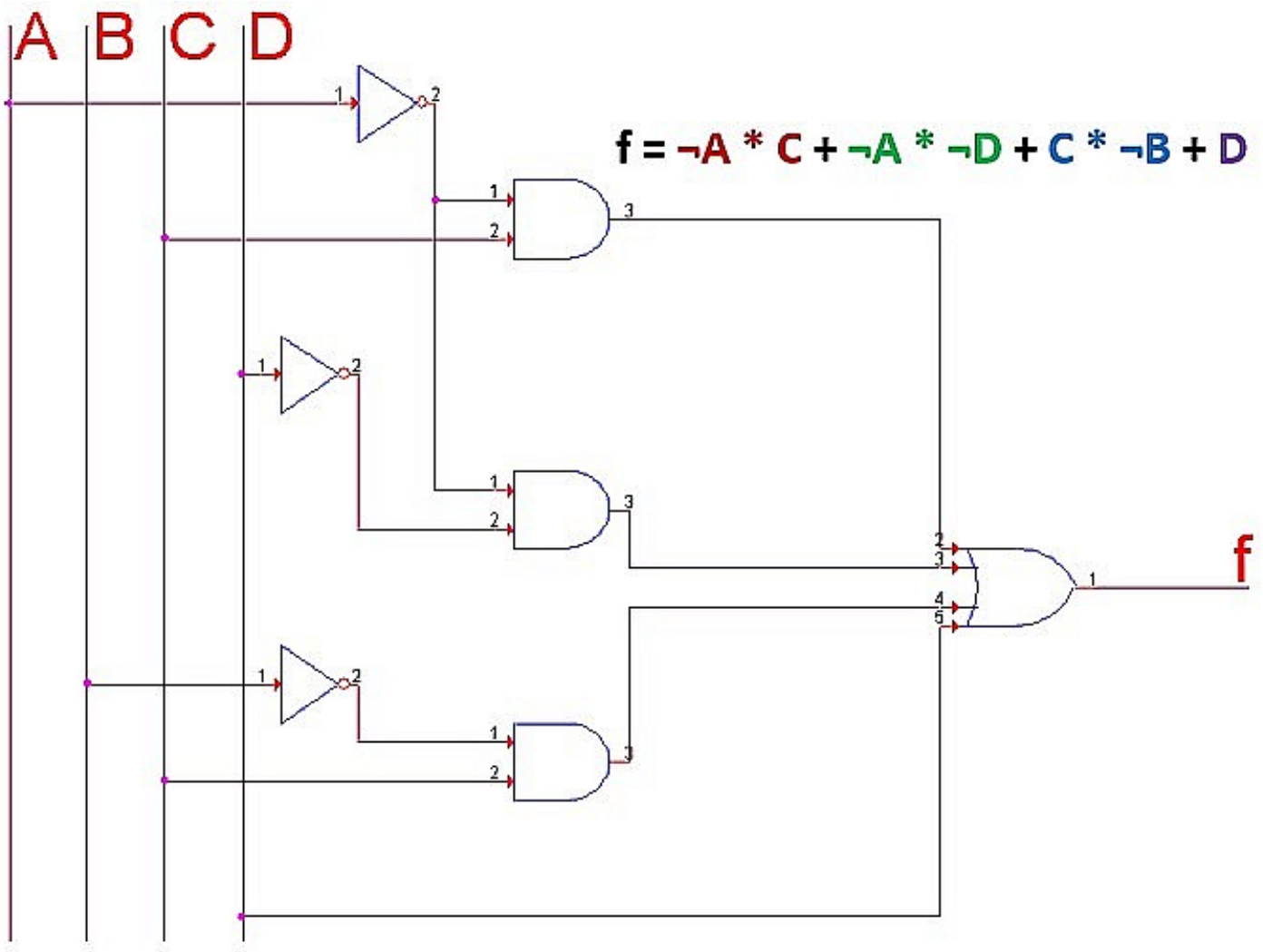
f = ¬A * C + ¬A * ¬D + C * ¬B

Beispiel: 7-segment-Anzeige



$$f = \neg A * C + \neg A * \neg D + C * \neg B + D$$

Beispiel: 7-segment-Anzeige



Vielen Dank

für Eure

Aufmerksamkeit!!

=)

Quellen

- cmos foto: http://www.google.de/imgres?imgurl=http%3A%2F%2Fwww.twistywristarcade.com%2Fc%2F12-category%2F4000-series-cmos-.jpg&imgrefurl=http%3A%2F%2Fwww.twistywristarcade.com%2F12-4000-series-cmos-&h=150&w=500&tbnid=Hy6R0Tu1yI98xM%3A&zoom=1&docid=bpZTveb6VBqOyM&ei=qlxeVLK6J42rPKuYgZgI&tbm=isch&client=firefox-a&iact=rc&uact=3&dur=1730&page=3&start=47&ndsp=28&ved=0COgBEK0DMEA
- temperaturtabelle/7400: http://de.wikipedia.org/wiki/Logikfamilie
- ideal/real: http://books.google.de/books?id=UEApBAAAQBAJ&pg=PA34&lpg=PA34&dq=ideale+und+reale+und+gatter&source=bl&ots=vjJT80xqoG&sig=_l6E0nYi25fpBv1wWOrHlLWMX0g&hl=de&sa=X&ei=cfNdVN-fDMKCPfO6gdgL&ved=0CDYQ6AEwBA#v=onepage&q&f=false
- logikfamilien: http://www.techniklexikon.net/d/logikfamilien/logikfamilien.htm
- http://www.dieelektronikerseite.de/Lections/Logikfamilien%20-%20Gleich%20und%20doch%20verschieden.htm
- http://www.uni-protokolle.de/Lexikon/Logikfamilie.html
- http://www.mikrocontroller.net/articles/74xx
- http://books.google.de/books?id=yL8hBAAAQBAJ&pg=PA509&lpg=PA509&dq=gatterlaufzeit+inverter&source=bl&ots=MQ58Ff8o4k&sig=XL2qgUZFDOB8EzN8LVbov3ViVVA&hl=de&sa=X&ei=3vxdVMeaFsLJOcilgNgC&ved=0CFEQ6AEwBA#v=onepage&q=gatterlaufzeit%20inverter&f=fals
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